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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/738,397	12/17/2003	Seung Woo Jin	CU-3496	7994

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EXAMINER	
TRAN, BINH X	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 08/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/738,397	JIN ET AL.	
	Examiner	Art Unit	
	Binh X. Tran	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) *7 and 15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-15* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02-09-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Species A (claims 1-6, 8-14) in the reply filed on 7-20-2006 is acknowledged. The traversal is on the ground(s) that "if the generic linking claims 1 and/or 2 are finally held allowance, those withdrawn claims that depend form the generic claim linking claims 1 and/or 2 should be reinstate and allows in the same application". This is not found persuasive because applicants fail to show that Species A and Species B are not distinct.

2. Further, the examiner clearly recognize that if the generic claim 1 or 2 is/are allowed, the restriction requirement as to the encompassed species would be withdrawn and claims 7 and 15, directed to the species of B would be no longer withdrawn from consideration if all of the claims to this species (i.e. 7 and 15) depend from or otherwise include each of the limitations of an allowed generic claim. However, at the present time, the generic claim 1 or 2 is not allowed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Kim (US 2002/0192868 A1).

Respect to claim 1, Kim discloses a method for fabricating a semiconductor device, comprising the steps of:

forming a gate line (105) on a semiconductor substrate (Fig 11);

forming a buffering layer (111) and a spacer nitride film (107) on the entire surface of the substrate including the gate line (paragraph 0043);

selectively etching the buffer layer (111) and the spacer nitride film (107) in such a manner that they remain on both sides of the gate line (Fig 12, paragraph 0043);

performing an ion implantation process using the remaining buffer and spacer nitride film as a barrier film to form junction regions (source/drain region 115) in the semiconductor substrate at both sides of the gate lines (105) (See Fig 13-14, paragraph 0044-0045);

forming an interlayer insulating film (119) on the entire upper portion of the result substrate (Fig 17);

selectively remove the interlayer insulating film (119) to form contact holes (139) exposing the upper surface of the junction region (Fig 17, paragraph 048);

forming a contact plug in the contact hole (paragraph 0052).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

> invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 2-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Akamatsu et al. (US 6,180,472).

Respect to claim 2, Kim fails to disclose the step of subjecting the entire upper portion of the substrate includes the junctions regions to a rapid thermal annealing (RTA) process, before the step of forming the interlayer insulating film. However, Kim clearly teaches to perform implantation process (i.e. doping process) to form the junctions region. Akamatsu teaches to a rapid thermal annealing process after the doping step and before the step of forming the interlayer insulating film in order to activate the dopants into the junction regions (i.e. source and drain region) (See col. 10 lines 1-33). It would have been obvious to one having ordinary skill in the art, at the time of the invention, to modify Kim in view of Akamatsu by performing a rapid thermal annealing process because it help to activate the dopants introduced into the junction regions.

Respect to claim 3, Kim discloses the buffer layer (111) is a single layer oxide film (paragraph 0032, 0043). Respect to claim 4, Kim discloses the spacer nitride film (107) is formed to a thickness of several hundreds angstroms (paragraph 0043, read on applicant's range).

Respect to claims 5-6, Kim fails to disclose that the ion implantation process is performed using a given tilt angle and a given number of rotations (claim 5); or the tilts angle is at 0-30 ° and the number of rotations is 2 to 4 (claim 6). However, Kim clearly teaches the step of ion implantation. Akamatsu teaches to perform ion implantation process two times (read on number of rotations is 2) at the tilt angle 7 ° to 40 ° to form heavily doped source/drain region (9) and lightly-doped region (col. 10 lines 1-45). It would have been obvious to one having ordinary skill in the art, at the time of the invention, to modify Kim in view Akamatsu by perform an ion implantation process having a given till angle and given number of rotations because it helps to form heavily doped source/drain region and lightly-doped source/drain region.

8. Claims 8, 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Okita (US 2003/0155595 A1).

Respect to claim 8, Kim fails to disclose the step of performing a rapid thermal annealing (RTA) process after the step of forming the interlayer insulating film. However, Kim clearly teaches to form the interlayer insulating film (119). Okita teaches to perform a rapid thermal annealing process after forming interlayer insulating layer (8) to prevent peeling-off of the conductive material (paragraph 0060). It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Kim in

view of Okita by performing RTA because this process will prevent peeling-off conductive material deposited on the interlayer insulating film.

The limitation of claims 11-12 has been discussed above under Kim's reference (See discussion of claims 3-4).

9. Claims 9, 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Gupta et al. (US 6,747,294).

Respect to claim 9, Kim fails to disclose subjecting the interlayer insulating film to a reflow annealing process and a rapid thermal annealing process after the step of forming the interlayer insulating film. However, Kim clearly discloses the step of forming interlayer insulating film (119) and planarizing the insulating film (119) (paragraph 0048). Gupta discloses the forming a planarization film made of dielectric material (read on interlayer insulating film) to provide a smooth surface for the circuit. Gupta further discloses the step of reflow annealing and rapid thermal annealing the interlayer insulating film in order to improve dopants activation (col. 6 lines 25-33). It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Kim in view of Gupta by performing reflow annealing and rapid thermal annealing because these process will help to improve dopants activation.

The limitation of claims 11-12 has been discussed above under Kim's reference (See discussion of claims 3-4).

10. Claims 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Akamatsu (US 6,180,472) and further in view of Okita (US 2003/0155595).

Respect to claim 10, Kim fails to disclose the step of performing a high temperature rapid thermal annealing process before forming the contacts plug. Akamatsu teaches to performing a high temperature (i.e. 900-1000 °C) rapid thermal annealing (RTA) process before forming the contacts plug (11) in order to activate dopants (See col. 5 lines 1-7, and lines 42-45). It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Kim in view of Akamatsu by performing a high temperature RTA process before forming the contact plugs because it help to activate dopants.

Respect to claim 10, Kim and Akamatsu fail to disclose a low temperature RTA process after forming the contact plugs. Okita teaches to perform a low temperature (600-750 °C) RTA process after the step of forming a contact plugs (See paragraph 0057-0060). It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Kim and Akamatsu by performing a low RTA process after the step of forming the contact plug because it will prevent peeling-off conductive material.

The limitation of claims 11-12 has been discussed above under Kim's reference (See discussion of claims 3-4). The limitation of claims 13-14 has been discussed above under Akamatsu's reference (See discussion of claims 5-6).

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh X. Tran whose telephone number is (571) 272-

1469. The examiner can normally be reached on Monday-Thursday and every other Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Binh Tran

Binh X. Tran